

Development of Ku-band Receiver/Downconverter for Satellite Transponders

Jin-Cheol Jeong, Yong Hei Lim, Byung-Jun Jang, In-Bok Yom, Seong-Pal Lee

Communications Satellite Development Center
ETRI-Radio & Broadcasting Technology Laboratory
161 Kajong-Dong, Yusong-Gu, Taejon, 305-350, KOREA

TEL : +82-42-860-6422, Fax : +82-42-860-6949, E-mail : jcjung@etri.re.kr

Abstract — This paper presents the development of a Ku-band Receiver/Downconverter with the Noise figure of 1.83dBmax and the conversion gain of 55dB at the frequency range from 14~14.5GHz to 12.252~12.752GHz for Ku-band Satellite transponders. This Ku-band Receiver/Downconverter consists of a LNA module, a 2-pole combine image rejection filter, a Downconverter module, a 7-pole IF filter, and an IFAMP module. All components except the cavity type filters were assembled using a hybrid technology with 15-mil thin-film substrates. Its other performances show the C/IM3 of 45.67dBmax, group delay of 0.6 ns/36MHz, and gain variation of 1.68 dBmax at $-15^{\circ}\text{C} \sim +65^{\circ}\text{C}$ of operating temperature range.

I. INTRODUCTION

The linearity, good temperature stability, and low noise figure are key performance parameters of the Receiver/Downconverter for satellite transponders. This paper describes the development of the Ku-band Receiver/Downconverter from the input frequency 14~14.5GHz, to the output frequency, 12.252~12.752GHz for Satellite transponders. All RF components were assembled using a hybrid technology with 15-mil thin-film substrate. The Receiver/Downconverter equipment consists of a low noise amplifier module, a downconverter module driven from a local oscillator which was excepted in our development, and an IFAMP module as shown in Fig.1. The input and output of the Receiver/Downconverter module provide the waveguide interface and coaxial output port, respectively. The test results of the Receiver/Downconverter were 55dB gain, 1.83dBmax Noise figure, 45.67dBmax C/IM3, 0.6ns/36MHz group delay, and 1.68 dBmax gain variation at $-15^{\circ}\text{C} \sim +65^{\circ}\text{C}$ of operating temperature range.

II. DESIGN OF RECEIVER/DOWNCONVERTER

A. LNA module design

The LNA module consists of an Iso-transition, 3-stage

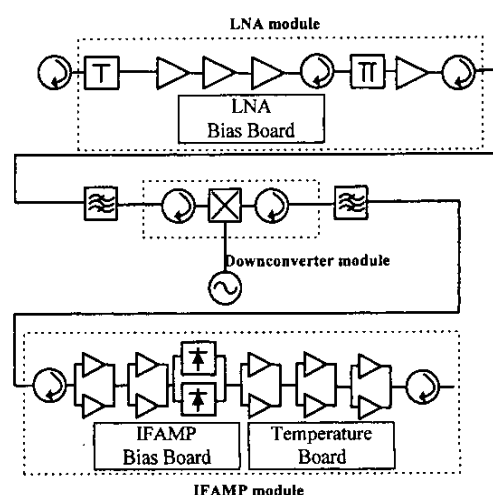
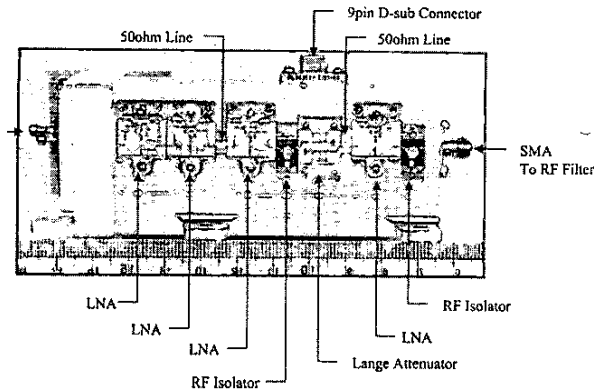


Fig.1. Functional block diagram of the Ku-band Receiver/Downconverter.

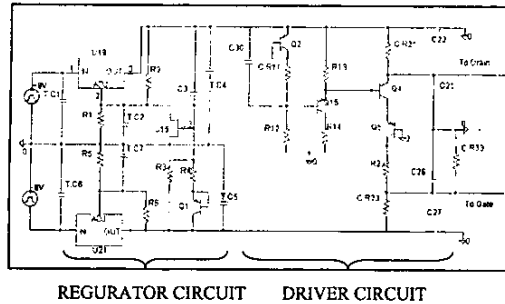
low noise amplifier, a fixed attenuator for gain level control, a single stage low noise amplifier, and a drop-in Isolator for improving the VSWR.

The transition of waveguide (WR75) to microstrip line was designed using the 3D EM simulator(HFSS) to have a maximum return loss. Four gain stages are four identical single stage and noise-matched amplifiers based on 0.15 μm Fujitsu (FHR20x) p-HEMT chip. The gain and noise figure of each stage were 8.5 dB and 1.1 dB, respectively. The fixed attenuator is a balanced type attenuator with Lange coupler. It has three ports with resistors at their end side. The attenuator provides the required gain of the Receiver/Downconverter and avoids too high power level into the following mixer in the downconverter module. The attenuator is initially set to 1 dB but can be controlled by 1 dB to 8 dB by each port connections. DC bias circuit driving the LNA consists of the regulator circuit with the negative voltage pre-apply circuit and driving circuit. Its supply biases are 2V of drain voltage and 5mA of drain

current for each stage LNA. Fig.2 (a) and (b) show the RF side of the LNA module and DC bias circuit.



(a) RF side picture of the LNA module



(b) DC bias circuit

Fig. 2. LNA module configure

B. Downconverter module design

The Downconverter module consists of a mixer and two drop-in Isolators for improving of In/Out VSWR. The mixer was designed with the configuration of double balanced type using HSCH9201 series diodes. For the design of the RF and LO baluns, the ring coupler and branch line coupler followed by 90 degree line were used, respectively. The mixing products at the 12GHz IF port, in specially 7LO(12.236GHz), can cause a serious problem at the spurious requirement of the receiver/downconverter [1],[2]. For minimizing the LO harmonics, we used the LO harmonic termination at the mixer design with the $1/4\lambda$ open-stub.

C. Filter design

The filters are required to provide levels of rejection of the image band at 11 GHz for the image rejection filter, and in the 14 GHz receive band at other frequencies close to band for the IF filter.

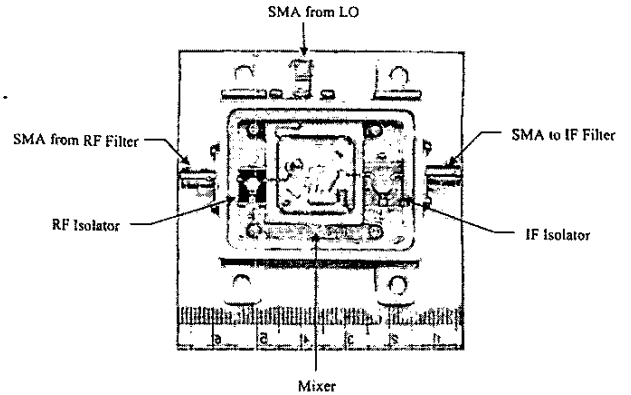


Fig. 3. Downconverter module

Compact filters of low mass and small size are required in this position. MIC type filters were considered but prove to have poor isolation out of band frequency. Coaxial combline filters with resonators of one eighth of a wavelength lend themselves to compact realizations with good wide band performance achievable [3]. Analysis of the requirements indicated that a 2 pole design for the image rejection filter and 7 pole design for the IF filter satisfied the electrical requirements sufficiently. Fig. 4 (a) and (b) show the 2-pole image rejection filter and 7-pole IF filter, respectively.

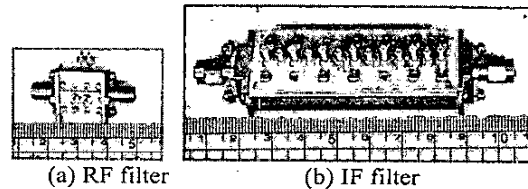


Fig. 4. Picture of the filters

D. IFAMP module design

The IFAMP module consists of 2-stage amplifier, a PIN attenuator for temperature compensation, 3-stage amplifier, and 2 drop-in Isolator for improving the VSWR. Fig. 5 (a) shows the photograph of the IFAMP RF side. Both two stage amplifiers front and rear the PIN attenuator are balanced type and gain matched amplifiers using the Fujitsu FHX35x 0.25 μm HEMT device. Each stage has a gain of 9 dB with 3 GHz usable bandwidth. The PIN attenuator is used to control the gain of the Receiver/ Downconverter RF chain. Together with a temperature sensor and PIN diode driver circuit, the PIN attenuator compensate for the variation of gain over temperature of the Receiver/Downconverter. The attenuator is a balance type PIN attenuator for a good VSWR with Alpha PIN(APD1510) diode. Compensation

is expected to require ± 4 dB variation over the qualification temperature range of $-15^{\circ}\text{C} \sim +65^{\circ}\text{C}$, well within the capability of the attenuator design.

The analog temperature compensation circuit driving the PIN attenuator is shown in Fig. 5 (b).

The output stage amplifier is a balanced type and power matched amplifier using FHX35x devices. It provides a good output power performance to meet the requirements for amplitude linearity with the third order intercept point of +28dBm.

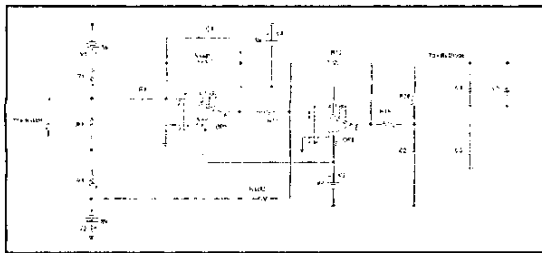
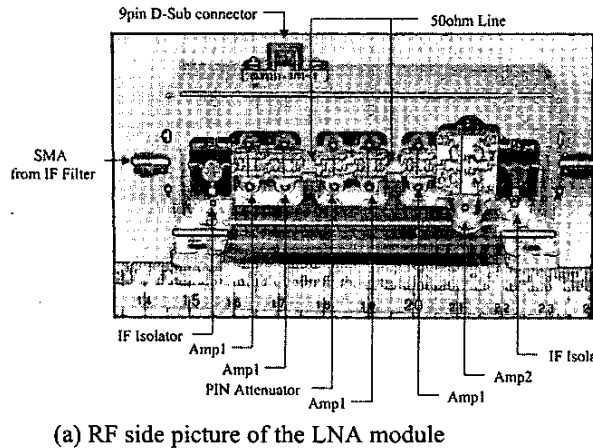


Fig. 5. IFAMP module configuration

III. MEASUREMENT OF RECEIVER/DOWNCONVERTER

Fig. 6. shows the measured conversion gain performance of the receiver/downconverter. For exact calibration of the used Scalar Network Analyzer (Marconi 8200B) and convenient measurement, 55dB fixed attenuator and additional RF cable were used. The conversion gain over the operating frequency range was $55 \text{ dB} \pm 0.8 \text{ dB}$ at ambient temperature. Over any 36 MHz band, the gain did not vary more than 0.3 dB. The gain slope at any operating frequency did not exceed 0.01 dB/MHz

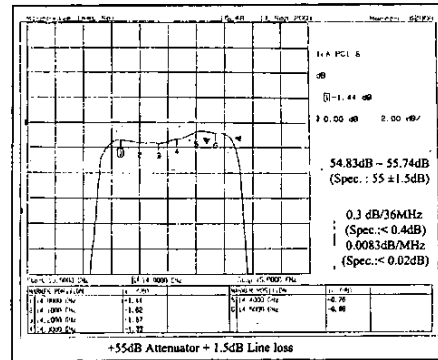


Fig. 6. Measured conversion gain performance

Fig. 7. shows the temperature performance of the conversion gain at the temperature range of $-15^{\circ}\text{C} \sim +65^{\circ}\text{C}$. The maximum gain variation at any specific frequency within the operating frequency range in the operating temperature was 1.6 dBp-p.

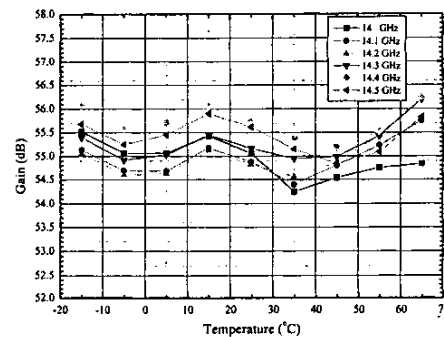


Fig. 7. Temperature performance of the conversion gain

Fig. 8. shows the noise figure performance of the Receiver/Downconverter. The maximum noise figure over the operating frequency range was 1.83dB at ambient temperature.

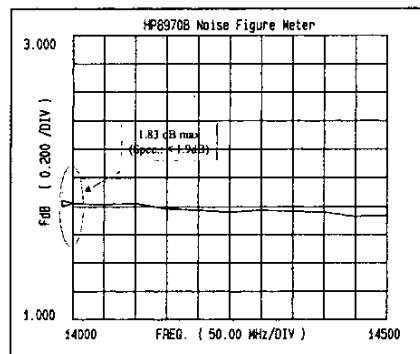


Fig. 8. Noise figure performance of the Receiver/Downconverter

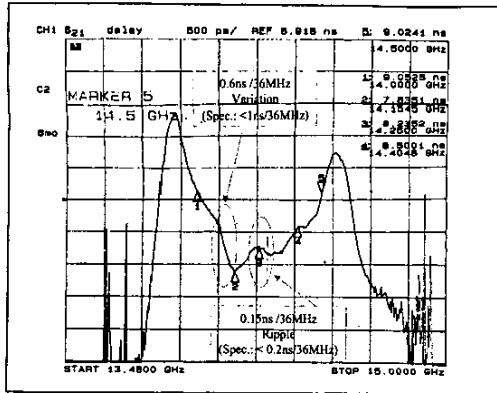


Fig. 9. Group delay performance

Fig. 9. shows the group delay performance. The group delay variation in any 36 MHz band within the range of the operating frequency did not exceed 0.6 ns p-p. The group delay ripple for any 36 MHz band did not exceed 0.15 ns p-p.

With two carriers each at input level of -53 dBm and 4MHz separation, the carrier to the third order Intermodulation ratio (C/IM_3) was 45.67dBc. Fig. 10. shows the IMD performance of the Receiver/Downconverter.

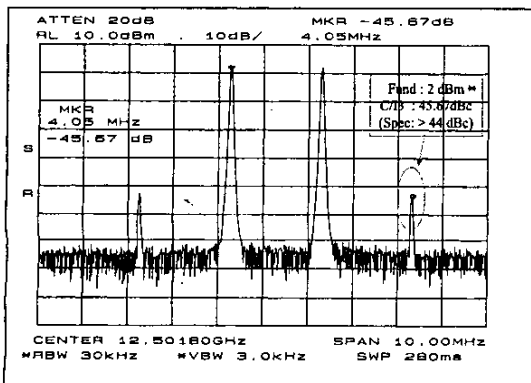


Fig. 10. IMD performance

Fig.11. shows the out-of-band spurious performance of 7LO harmonic. Due to too near apart (16MHz) from the operating frequency range, its spurious performance can be a serious problem at the system operation. The measured result shows the 18.5dBm of the 7LO harmonic power. Considering the IFAMP module gain of about 40 dB and the fundamental LO power of +13dBm, we can calculate the 7LO harmonic compression for 1LO is about 71.5dBc.

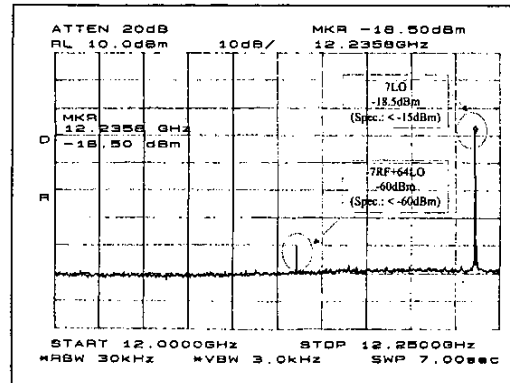


Fig. 11. Out of band spurious performance

IV. CONCLUSION

This paper describes the development of the Ku-band Receiver/Downconverter with the frequency range from 14~14.5GHz to 12.252~12.752GHz for Satellite transponders. The test results for the Receiver/Downconverter were 55dB gain, 1.83dBmax noise figure, 45.67dBcmax C/IM_3 , 0.6ns/36MHz group delay, and 1.68 dBmax gain variation for $-15^{\circ}\text{C} \sim +65^{\circ}\text{C}$ of operating temperature range. Nearly all measured results comply the requirements for the Receiver/Downconverter for Satellite transponders.

ACKNOWLEDGEMENT

The authors wish to acknowledge the assistance and support of the Satellite RF team members at ETRI.

REFERENCES

- [1] Itoh K, Kawakami K, Kamikokura A, Iida A, Ishida O, Betsudan S, "A drain mixer with low spuriousness for satellite transponders," *Electronics & Communications in Japan, Part 2: Electronics (English Translation of Denshi Tsushin Gakkai Ronbunshi)*, vol.80, no.12, pp.37-49, Dec. 1997.
- [2] A. Suriani, P. Montanucci, P. Ranieri, "Design of Microstrip Balanced Mixers for Spurious Outputs Suppression in Ku band Satellite repeaters," *Microwave Conference and Exhibition, 27th European*, vol 2, pp. 1076-1079, Sep. 1997.
- [3] In-Bok Yom, Kun-Wook Chung, Kwang-Ryang Park, Jae-Moung Kim, "Design of direct coupled combline filter with tapped line in/output for Ku-band satellite transponder downconverter," *Journal of the Institute of Electronics Engineers of Korea D*, vol.34-D, no.12, pp.22-30, Dec. 1997.